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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,666	03/18/2004	Chung-Chin Shih	12423-US-PA-X-0P	2665

31561 7590 10/18/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
OWENS, DOUGLAS W	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,666	SHIH, CHUNG-CHIN	
	Examiner	Art Unit	
	Douglas W. Owens	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-22* is/are allowed.

6)☒ Claim(s) *1,2,5-8,10 and 12* is/are rejected.

7)☒ Claim(s) *3,4,9 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 5, 6, 8, 10 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,835,987 to Yaegashi.

Regarding claim 1, Yaegashi teaches a memory device (Figs. 6 – 11 and 18, for example), comprising:

a plurality of isolation regions (17) disposed in a substrate (1), defining a plurality of active regions (16) in the substrate;

a plurality of pairs of word lines (14, in gate stacks 18) substantially parallel to one another, disposed on and in a direction vertical to the plurality of isolation structures and the plurality of active regions, wherein the active regions that are covered by the plurality of pairs of word lines are defined as a plurality of first channel regions;

a plurality of first gates (11) disposed on the plurality of the first channel regions and between the substrate and the plurality of word lines;

a plurality of pairs of source lines (14 of gate stacks 19), substantially parallel to the plurality of pairs of word lines, each pair of source lines being between each pair of

word lines, wherein the plurality of source lines are disposed in a direction vertical to the plurality of isolation structures and the plurality of active regions, and wherein the active regions that are covered by the plurality of pairs of source lines are defined as a plurality of second channel regions;

a plurality of second gates (11), in strip shapes, disposed on an in a direction vertical to the plurality of isolation structures and the plurality of the active regions and between the substrate and the plurality of source lines;

a first dielectric layer (5) between the plurality of active regions and the plurality of first gates, and between the plurality of active regions and the plurality of second gates;

a second dielectric layer (13) between the plurality of word lines and the plurality of first gates and between the plurality of sources lines and the plurality of second gates;

a third dielectric layer (25) disposed over the substrate and covering the plurality of word lines and the plurality of source lines;

a plurality of source/drain regions (23, 24) disposed in the active regions beside the first gates and the second gates;

a plurality of source line contacts (Fig. 18; Col. 14, lines 31 – 40), through the third dielectric layer, connecting to the source/drain regions that are between each pair of the source lines and electrically connecting to at least one of each pair of source lines; and

a plurality of insulating layers (20) disposed between the plurality of the second gates and the plurality of the source line contacts.

Regarding claim 2, Yaegashi teaches a memory device, wherein the plurality of isolation structures are disposed in strip shapes, thus defining the active regions in strip shapes.

Regarding claim 5, Yaegashi teaches a memory device, wherein the material of the source lines is the same as that of the word lines (Col. 11, lines 60 and 61).

Regarding claim 6, Yaegashi teaches a memory device, wherein the material of the source lines and word lines include polysilicon and metal silicide (Col. 11, lines 60 and 61).

Regarding claim 8, Yaegashi teaches a memory device, wherein each source line contact connects to one source/drain region and electrically connects to at least one of each pair of the source lines.

Regarding claim 10, Yaegashi teaches a memory device, wherein each source line contact is a self-aligned contact.

Regarding claim 12, Yaegashi teaches a memory device, wherein the memory device is a flash memory device, the first gate is a floating gate and the second gate is a select gate.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yaegashi. Yaegashi teaches a memory device, further comprising a plurality of spacers (29, 33). Yaegashi does not teach that the thickness of the insulating layer between the second gate and the source line contact is smaller than half of a thickness of the spacer. The thickness of the insulation layer between a floating gate and control gate is a known result effective variable that is subject to optimization. It would have been obvious to one of ordinary skill in the art to find the optimal thickness thereof through routine experimentation (*In re Antonie*, 559 F.2d 618, 195 USPQ 6 (CCPA 1977)).

Allowable Subject Matter

5. Claims 3, 4, 9 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 13 – 22 are allowed.

Response to Arguments

7. Applicant's arguments filed August 4, 2005 have been fully considered but they are not persuasive.

Applicant argues that Yaegashi fails to teach a memory device including "a plurality of pairs of source lines, substantially parallel to the plurality of word lines." This feature can be seen in Figs. 7 and 8, where the pairs of source lines (14) in the selection gate stacks (19) are parallel to the plurality of word lines (also 14, but in a different gate stack) in the memory gate stacks (18). Note that the same terminology

that the Applicant has used to refer to the source lines (215a, 215b) and word lines (214a, 214b) (control gates in Applicant's Fig. 3B, for example) has been used to refer to the same structures in the device taught by Yaegashi (See Fig. 8). Although the language is different, the structure is identical. It can be seen in Fig. 7, that the source lines and word lines are parallel. In other words, in the instant application the control gate of the select transistor is referred to as the "source line" and the control gate of the memory transistor is referred to as the word line. This is the structure taught by Yaegashi.

Applicant argues that the Examiner used the same gate to show two different gates. The claim requires "a plurality of first gates disposed on the plurality of the first channel regions and between the substrate and the plurality of word lines" and "a plurality of second gates, in strip shapes, disposed on an in a direction vertical to the plurality of isolation structures and the plurality of the active regions and between the substrate and the plurality of source lines." Since two gates are enough to constitute a plurality of gates, the first gates on the plurality of first channel regions are the two gates (11) in gate stacks 18. The plurality of second gates (11) are disposed in gate stacks 19.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven H. Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Douglas W Owens
Examiner
Art Unit 2811